U.S. Application Serial No. 09/800,851
Declaration dated July 14, 2004
Filed with Reply to Office Action of March 15, 2004

Attorney Docket No.: 10006513-1 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	John F. Hutton et al.	Examiner:	Albert C. WANG
Serial No.:	09/800,851	Art Unit:	2115
Filed:	March 7, 2001		
For:	A SCAN BASED MULTIPLE RING OSCILLATOR STRUCTURE FOR ON-CHIP SPEED MEASUREMENT		

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

DECLARATION OF JOHN F. HUTTON PURSUANT TO 37 C.F.R. § 1.131

Dear Sir:

1. Prior to December 28, 2000, the filing date of US Patent No. 6,535,013 to Samaan, I jointly conceived of at least a method for detecting process variations comprising controlling count gate control by a first circuit, generating at least one clock count by a second circuit, and outputting results of the clock count by a third circuit, as claimed in claims 1-9 of the present application.

2. Prior to December 28, 2000, I jointly conceived of at least an apparatus to detect process variations comprising a first circuit to select a clock, a second circuit connected to the first circuit to generate at least one clock count, and a third circuit connected to the first circuit to output a result of the clock count, as claimed in claims 10-20 of the present application.

3. On August 15, 2000, I jointly submitted an Invention Disclosure form to Hewlett-Packard's internal Legal Department (HP Legal). *See* Exhibit A. The Invention Disclosure form that I submitted included the brief description and diagrams associated with the invention. Such Invention Disclosure forms are submitted so that HP Legal can determine whether to file a patent application.

4. From immediately prior to December 28, 2000 until the March 7, 2001, the effective filing date of the present application, the claimed invention was constructively reduced to practice with due diligence.

5. On December 28, 2000, I sent draft figures related to the claimed invention to Ami Shah, previously of Dorsey & Whitney LLP.

6. On or about February 4, 2001, I received a draft application describing the claimed invention from Ami Shah.

7. On or about February 6, 2001, I subsequently reviewed the draft application and provided comments to Ami Shah.

8. On or about February 8, 2001, I received a revised draft application describing the claimed invention from Ami Shah.

9. On or about February 21, 2001, I subsequently reviewed the revised draft application and provided comments and other feedback.

10. On March 7, 2001, the present application was filed.

11. The acts related above all took place in the United States of America.

12. The declarant further states that the above statements were made with the knowledge that willful false statements and the like are punishable by fine and/or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that any such willful false statement may jeopardize the validity of this application or any patent resulting therefrom.

Date: July 14, 2004

John F. Hutton

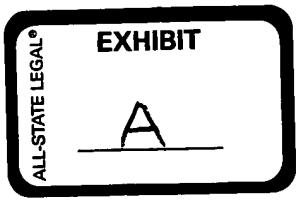
EXHIBIT
A
ALL-STATE LEGAL®

HEWLETT PACKARD

INVENTION DISCLOSURE

PDNO 10006513 DATE RCVD 8/15/00 PAGE ONE OF ____ ATTORNEY AJN VTC

*Instructions: The information contained in this document is **COMPANY CONFIDENTIAL** and may not be disclosed to others without prior authorization. Submit this disclosure to the HP Legal Department as soon as possible. No patent protection is possible until a patent application is authorized, prepared, and submitted to the Government.*

Descriptive Title of Invention:
Scan based multiple ring oscillator structure for on-chip spead measurement and coorelation

Name of Project: Piranha (PCXX? 8600?)

Product Name or Number:

Was a description of the invention published, or are you planning to publish? If so, the date(s) and publication(s):
No

Was a product including the invention announced, offered for sale, sold, or is such activity proposed? If so, the date(s) and location(s):
NO

Was the invention disclosed to anyone outside of HP, or will such disclosure occur? If so, the date(s) and name(s):
NO

If any of the above situations will occur within 3 months, call your IP attorney or the Legal Department now at: 1-858-4513 or 970-898-4919.

Was the invention described in a lab book or other record? If so, please identify (lab book #, etc.)
Yes - John Hutton's lab book

Was the invention built or tested? If so, the date:
Yes - on current release of piranha

Was this invention made under a government contract? If so, the agency and contract number:
NO

Description of Invention: *Please preserve all records of the invention and attach additional pages for the following. Each additional page should be signed and dated by the inventor(s) and witness(es).*

A. Prior solutions and their disadvantages (if available, attach copies of product literature, technical articles, patents, etc.).

SEE ATTACHMENT 0

B. Problems solved by the invention.

Attachment

C. Advantages of the invention over what has been done before.

Attachment

D. Description of the construction and operation of the invention (include appropriate schematic, block, & timing diagrams; drawings; samples; graphs; flowcharts; computer listings; test results; etc.)

Attachment

Signature of Inventor(s): Pursuant to my (our) employment agreement, I (we) submit this disclosure on:

Employee No.	Name	Signature	Telnet	Mailstop	Entity & Lab Name
243148	John F. Hutton	John F. Hutton	898-4497	88	VTC
315507	William A. Hudson	William A. Hudson	898-3458	88	VTC
315502	Daniel L. Halperin		898-3273	88	VTC
311897	Daniel W. Krueger		898-2236	88	VTC

(If more than four inventors, include additional information on another copy of this form and attach to this document)

Signature of Inventor(s): Pursuant to my (our) employment agreement, I (we) submit this disclosure on:

Employee No.	Name	Signature	Telnet	Mailstop	Entity & Lab Name
244155	Jack T. Lavier		898-0404	88	VTC
243034	Mark D. Musgrove		898-7895	88	VTC

(If more than four inventors, include additional information on another copy of this form and attach to this document)

HEWLETT-PACKARD **INVENTION DISCLOSURE** COMPANY CONFIDEN PAGE ___ OF ___

Signature of Witness(es): *(Please try to obtain the signature of the person(s) to whom invention was first disclosed.)*

The invention was first explained to, and understood by, me (us) on this date:

Full Name	Signature	Date of Signature
J. Robert Sims, III		15 Mar 2001
		Date of Signature
Full Name	Signature	

Inventor & Home Address Information: *(If more than four inventors, include addl. information on a copy of this form & attach to this document)*

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Citizenship: USA

HEWLETT-PACKARD **INVENTION DISCLOSURE** COMPANY CONFIDENTIAL PAGE ____ OF ____

Signature of Witness(es): *(Please try to obtain the signature of the person(s) to whom invention was first disclosed.)*

The invention was first explained to, and understood by, me (us) on this date: Date of Signature

Full Name Signature

Full Name Signature Date of Signature

Inventor & Home Address Information: *(If more than four inventors, include addl. information on a copy of this form & attach to this document)*

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Street

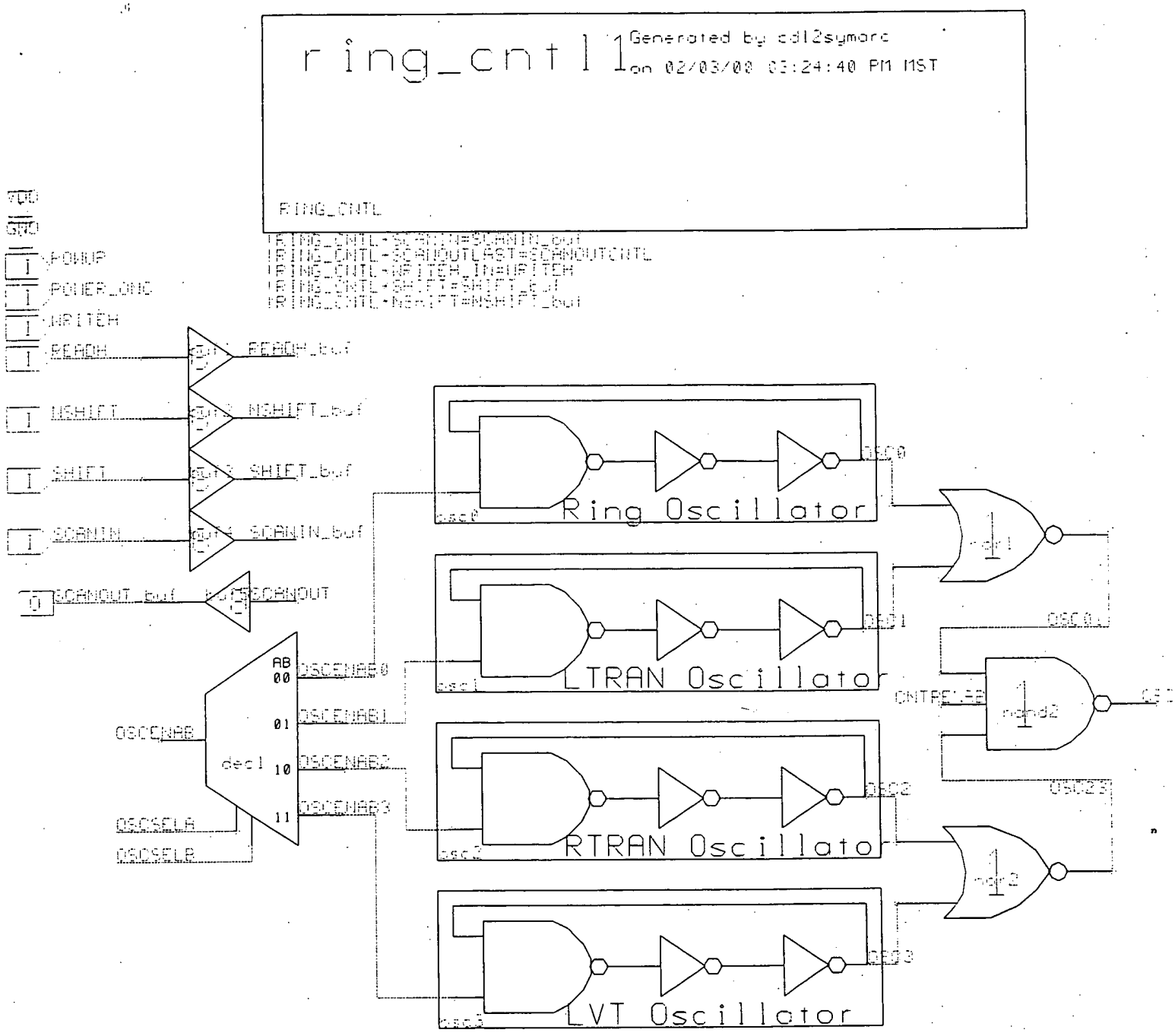
City

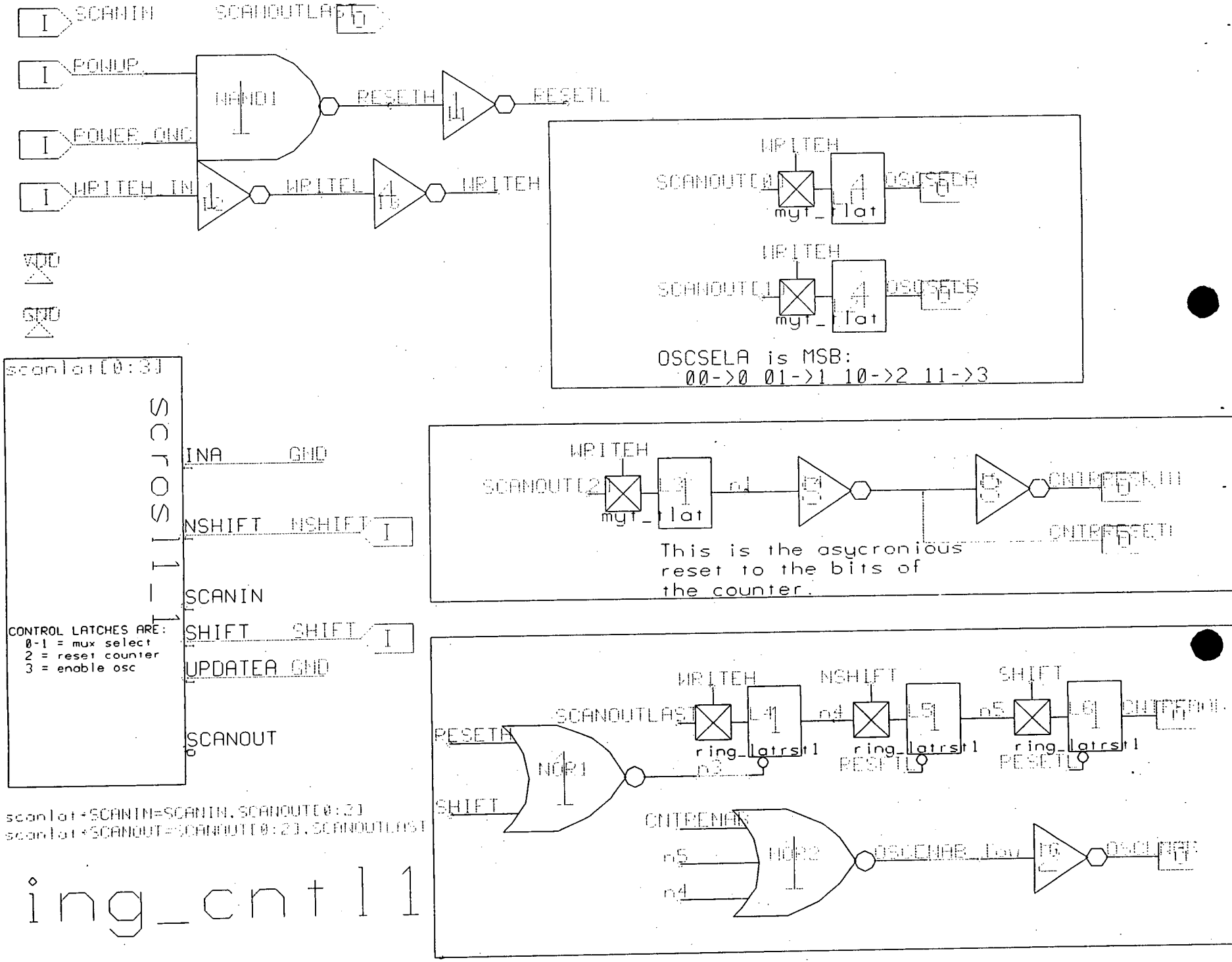
State Zip

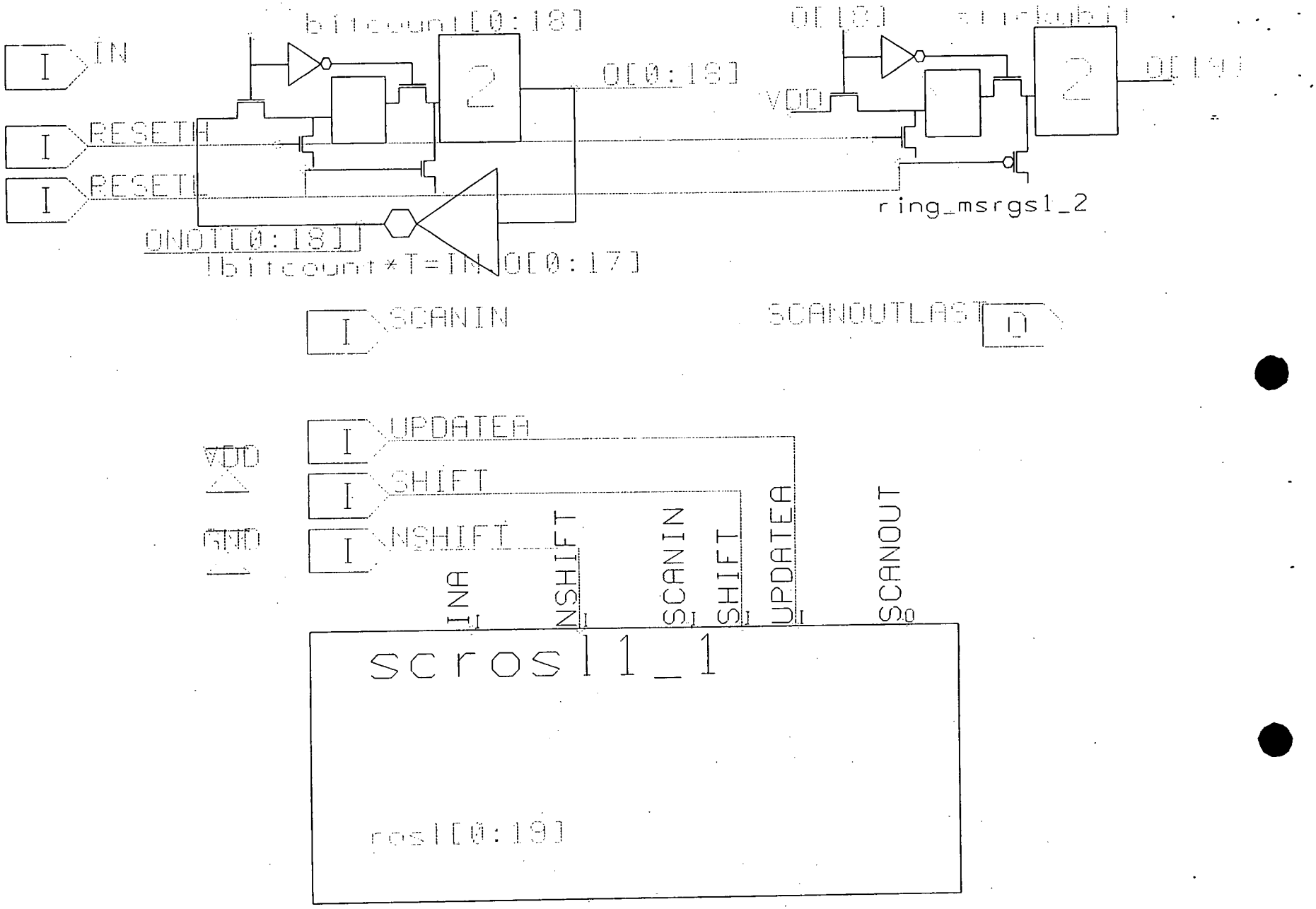
Do you have a Residential P.O. Address? P.O. BOX City State Zip

Greeted as *(nickname, middle name, etc.)*

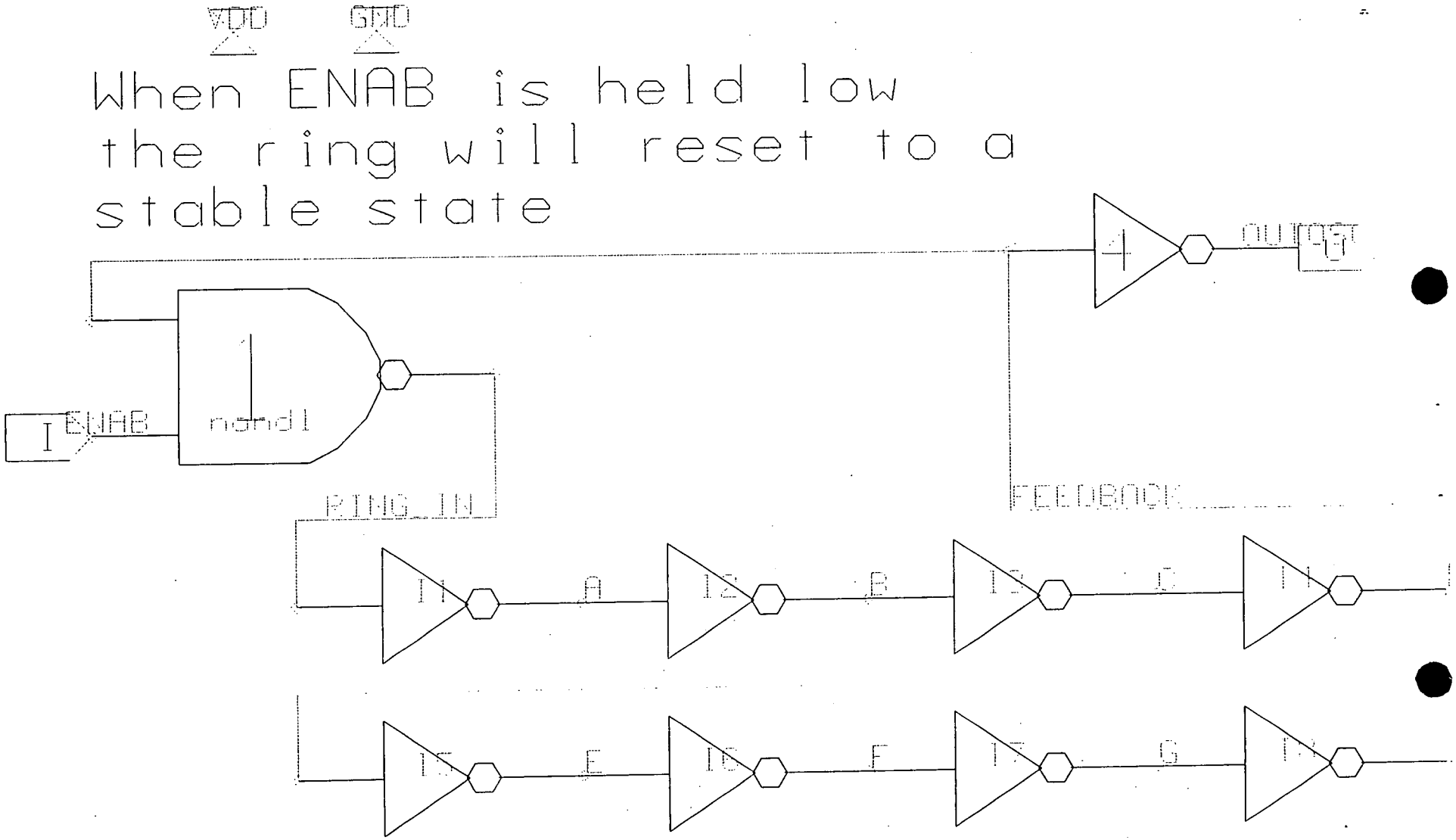
Citizenship


ring_cntl1
Generated by cdl2symarc
on 02/03/00 03:24:40 PM MST
RING_CNTL
!RING_CNTL-SCANIN=SCANIN_buf
!RING_CNTL-SCANOUTLAST=SCANOUTCNTL
!RING_CNTL-WRITEH_In=WRITEH
!RING_CNTL-SHIFT=SHIFT_buf
!RING_CNTL-NSHIFT=NSHIFT_buf
VDD
GND
PDNUP
POWER_ONC
WRITEH
READH
NSHIFT
SHIFT
SCANIN
SCANOUT_buf
READH_buf
NSHIFT_buf
SHIFT_buf
SCANIN_buf
SCANOUT
OSCENAB
OSCSELA
OSCSELB
decl
AB
00
01
10
11
OSCENAB0
OSCENAB1
OSCENAB2
OSCENAB3
Ring Oscillator
LTRAN Oscillator
RTRAN Oscillato
LVT Oscillator
OSC0
OSC1
OSC2
OSC3
CNTRESETB
OSC23
nand2
nor2
ring_counter1
Generated by cdl2symarc
on 01/10/00 01:42:53 PM MST
Scan Ports
Block Ports
RING_COUNTER
!RING_COUNTER-SCANIN=SCANOUTCNTL
!RING_COUNTER-SCANOUTLAST=SCANOUT
!RING_COUNTER-IN=OSC
!RING_COUNTER-UPDATEA=READH_buf
!RING_COUNTER-RESETH=CNTRESETH
!RING_COUNTER-RESETL=CNTRESETL
!RING_COUNTER-SHIFT=SHIFT_buf
!RING_COUNTER-NSHIFT=NSHIFT_buf
ring_block2

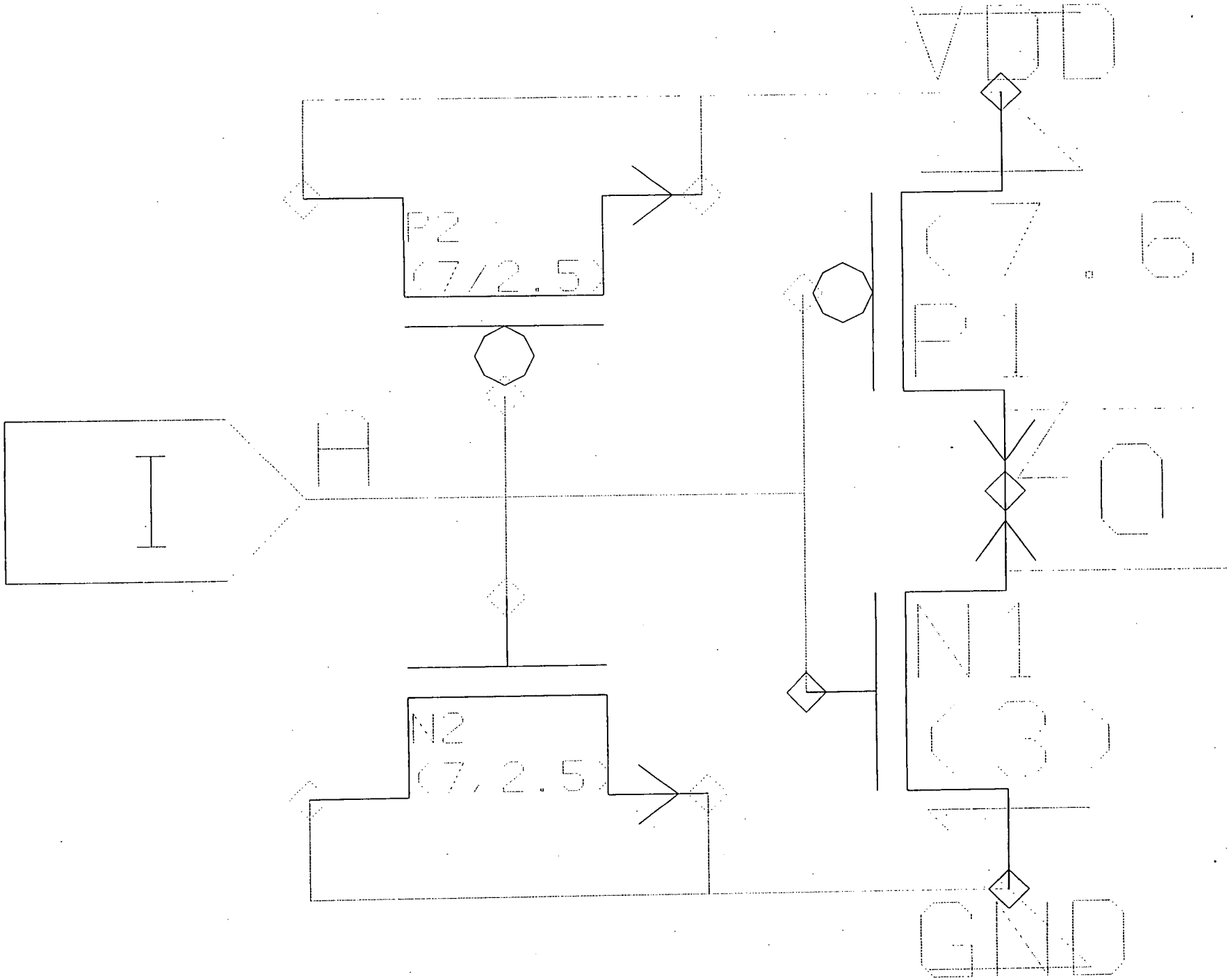

SCANIN
SCANOUTLAST
POWUP
NAND1
RESETH
RESETL
POWER_ONC
WRITEH_IN
WRITEL
WRITEH
VDD
GND
WRITEH
SCANOUT[0]
myt_flat
OSCSELA
WRITEH
SCANOUT[1]
myt_flat
OSCSELB
OSCSELA is MSB:
00->0 01->1 10->2 11->3
scanlat[0:3]
SCANLATCH
INA GND
NSHIFT NSHIFT
SCANIN
SHIFT SHIFT
UPDATEA GND
SCANOUT
CONTROL LATCHES ARE:
0-1 = mux select
2 = reset counter
3 = enable osc
!scanlat+SCANIN=SCANIN,SCANOUT[0:2]
!scanlat+SCANOUT=SCANOUT[0:2],SCANOUTLAST
WRITEH
SCANOUT[2]
myt_flat
n4
CNTRRESETH
CNTRRESETL
This is the asycronious
reset to the bits of
the counter.
WRITEH
NSHIFT
SHIFT
SCANOUTLAST
ring_latrstl
RESETL
RESETA
NOR1
n3
SHIFT
CNTRENAB
n5
n4
NOR2
OSCENAB_low
OSCI
ring_cntl1



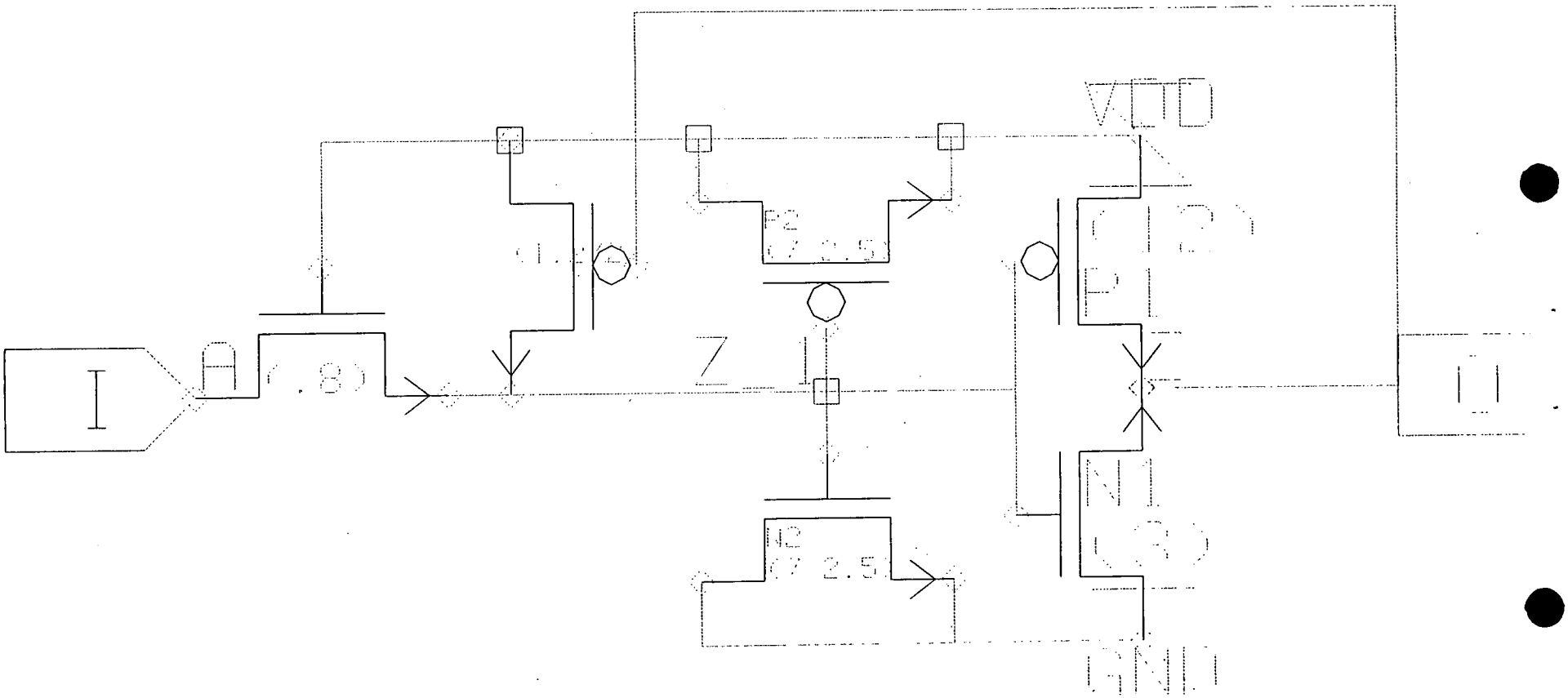
ring_counter1


VDD
GND
When ENAB is held low
the ring will reset to a
stable state
OUTPUT
ENAB
nsrdl
RING_IN
FEEDBACK
A
B
C
E
F
G

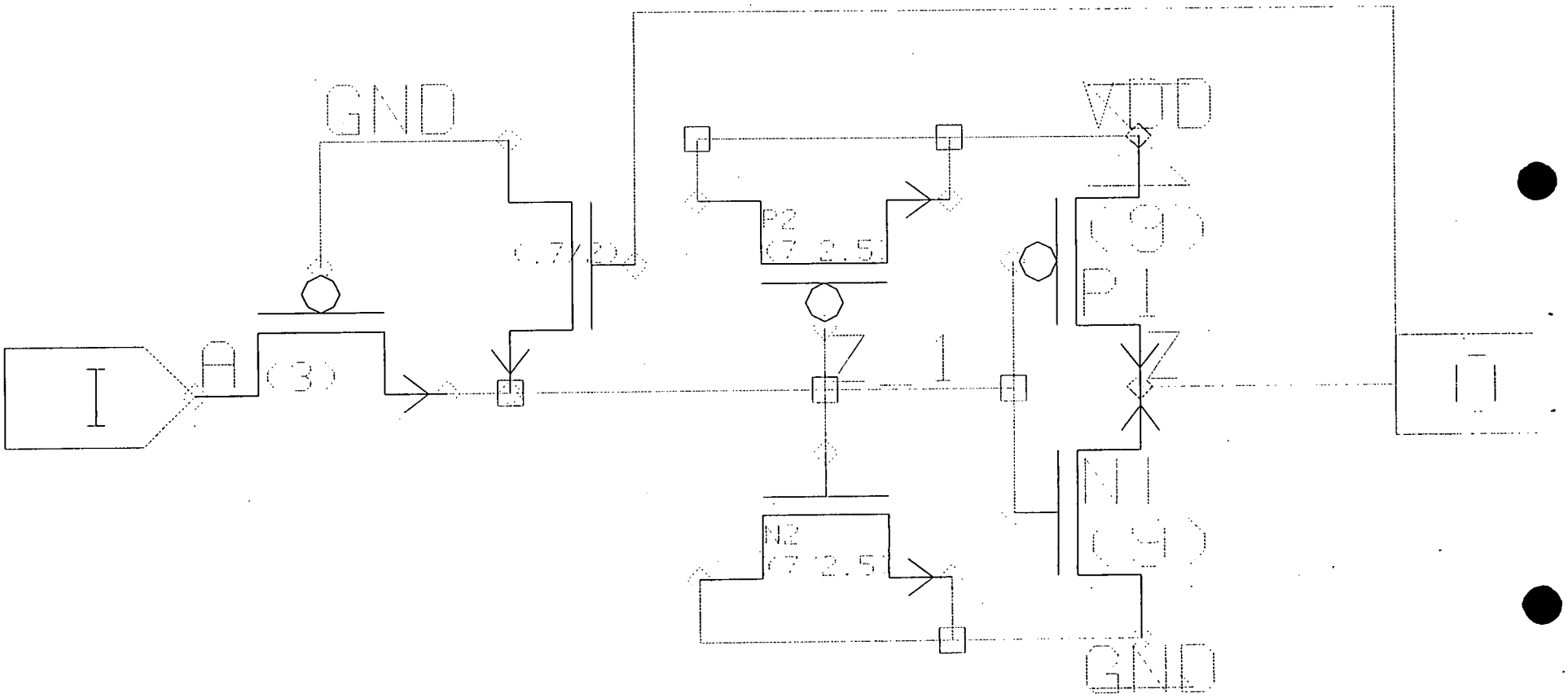
ring_osc1



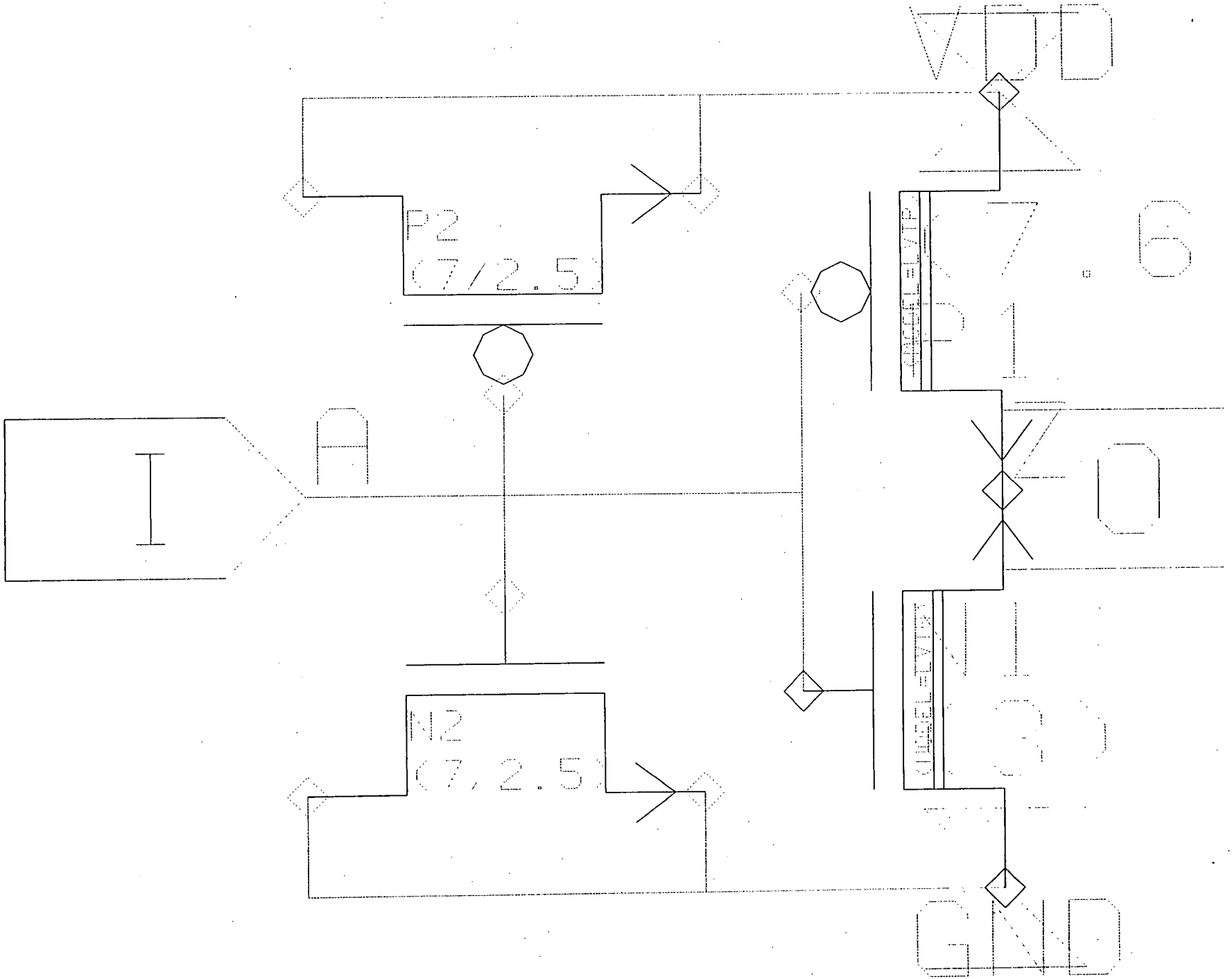
ring_inv1



ring_inv2



ring_invrtran1



ring_invlvt1

Alex -- Here is the bulk of my invention disclosure form with the schematic attachments. The form is attached as well as a slew of schematics from this block. Please let me know if you would like any more information.

Sincerely,

John Hutton
FML -- 3UP3, 0x84497, john_hutton@hp.com, jfh@fc.hp.com

-----X-----X-----X-----X-----X-----X-----X-----X-----X-----X-----X-----X-----

Ring Oscillator Invention Disclosure Form

Description of Invention

A. Prior solutions and their disadvantages

Speed binning is usually done based upon some type of broadside test done by a package tester. For piranha, the fuses that normally hold this information on the die are laser blowable, not electrically blowable. This means that some method to get a "best guess" at the speed of the part at wafer test will significantly reduce the price of packaging a part that will not make the frequency cutoff.

Some type of ring oscillators are ofter used in the analog parameter testing (APT) structures generated by the wafer manufacturer. However these tests are run by the fab which saves the information in a database. This does not help set the speed bin of the part at wafer test.

While I have heard of other ring oscillator structures (sadly no references) placed on a chip to attempt to compensate for process variation, I believe their affect was always to local circuits. They did not export their information outside of the chip.

B. Problems solved by this invention

This simple device bundles 4 ring oscillators, a 20-bit ripple counter, and the necessary control logic to a JTAG scan based interface. It is on every die, so that each location can be individually tested (APT sites tend to be scattered throughout the wafer). It communicates with the outside world through the standard JTAG interface. It is accessible at wafer, package, and system test which allows for several methods of correlating the oscillator speed to the speed of a part in an actual system. It is much simpler that a broadside test, and should directly track significant process variations.

C. Advantages

Simple. Tracks process. On every die. Accessible at wafer for early speed binning. Accessible through the wafer, package, and system test lifecycle which allows for accurate oscillator to system speed correlation.

D. Description of the construction and operation

This structure has three main parts: the oscillators, the counter, and the control. All of the relevant schematic and artwork plots will be attached to the end of this write-up.

The oscillators were build from simple fet structures. Each fet has a 'fet capacitor' type load to allow a reasonable frequency with a low number of stages. This also simulated a rise time on the order of 150 ps, which would be reasonable for a clock on this processor. The four oscillators are:

Normal oscillator, 8 stages, 800 MHz nominal frequency

LTran oscillator, added an N-fet pass transistor, 200 MHz nominal
RTran oscillator, added an P-fet pass transistor, 200 MHz nominal
Low Vt oscillator, the normal with Low Vt fets.

The L- and R-tran structure, at least in spice, had stronger dependences on the handedness of the process. We hope that this would allow us to keep better track of major process variations.

The counter was a simple 20-bit ripple counter with an asynchronous reset. It was composed of T-flip flops. While the ripple time was on the order of milliseconds, the scan control had no way of operating that fast. The danger of having an error related to ripple is almost non-existent.

The control is the heart of the structure. Since this circuit is entirely scan driven, we have to be able to reset, select one of the four oscillators, control the start and stop of the count, latch and scan out the final count. The 'start and stop' is the most critical segment of this block.

Two control bits select the oscillator. One control bit triggers a reset of the counter. The final bit is the enable line.

In order to accurately control the time that the counter is on, we set up a simple state machine that looks for two successive SHIFT-rising on the scan clock. This is a signal that the tester can control with a very high precision. The input scan vector disables the reset, selects the oscillator, and enables the count. On the next SHIFT clock, the counter is gated on. On the subsequent SHIFT clock, the counter is gated off. Then the count can be transfered back to the scan chain and shifted out.